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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,908	02/10/2004	Leonard Forbes	400.272US01	1212

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 10/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/775,908	FORBES, LEONARD	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 35-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 35-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's Amendment filed 10/13/2005 has been reviewed and placed of record in the file.

2. New (last) claim 42 has been renumbered 44.

3. Applicant's arguments with respect to amended claim 1 and to new claims 35-44, filed 10/13/2005, have been considered but they are moot in view of new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. **Claims 1, 36, and 38-40** are rejected under 35 U.S.C. 102(b) as being anticipated by Sadd et al. U.S. Patent Application Publication 20020076850 (hereinafter the '850 reference).

Referring to **claim 1**, the reference discloses an NROM memory transistor (paragraphs [0002 to [0011]], nonvolatile or nitride "read only memory" based on an improved SONOS structure) comprising:

a substrate (10) having a plurality of source/drain regions (not shown), the source/drain regions having a different conductivity type than the remainder of the substrate (as is known in the art);

a nanolaminate gate dielectric (20/30-50/60) formed on top of the substrate substantially between the plurality of source/drain regions, the gate dielectric comprising an oxide--nitride--high-k dielectric composition of oxide-nitride- Al_2O_3 (oxide-nitride-aluminum oxide, paragraphs [0012] to [0015]), meeting the claimed Markush group of oxide-nitride-Al_2O_3 and oxide-nitride-HfO_2; and

a control gate (70) formed on top of the gate dielectric.

Referring to **claim 36**, the reference further discloses that the control gate is a polysilicon material (paragraph [0016]).

Referring to **claims 38-40**, the limitations "fabricated using atomic layer deposition", "fabricated using an evaporation technique", and fabricated using a combination of an atomic layer deposition and an evaporation technique" are taken to be product-by-process limitations and considered non-limitation in a product claim (MPEP 2112.01 and MPEP 2113).

5. **Claims 1, 36, and 38-41** are rejected under 35 U.S.C. 102(e) as being anticipated by Mahajani et al. U.S. Patent Application Publication 20040069990 (hereinafter the '990 reference).

Referring to **claim 1**, the reference discloses an NROM memory transistor (paragraph [0042], nonvolatile or nitride "read only memory") comprising:

a substrate (not shown) having a plurality of source/drain regions (generally indicated at a portion of or adjacent to BL 15, Fig. 2, paragraph [0027]), the source/drain regions having a different conductivity type than the remainder of the substrate (as is known in the art);

a nanolaminate gate dielectric (5 including 13/11/9) formed on top of the substrate substantially between the plurality of source/drain regions, the gate dielectric comprising an oxide--nitride--high-k dielectric composition of oxide-nitride- Al_2O_3 (paragraphs [0018] to [0020]), meeting the claimed Markush group of oxide-nitride-Al_2O_3 and oxide-nitride-HfO_2; and

a control gate (3) formed on top of the gate dielectric.

Referring to **claim 41** and using the same reference characters, interpretations, and citations as detailed above for claim 1 where applicable, the reference discloses a non-volatile memory device comprising:

a memory array comprising a plurality of NROM memory transistors (paragraph [0042], nonvolatile or nitride "read only memory"), each transistor comprising:

a substrate (generally indicated at 108/3/101/lower-portion-of-device-level 102 including BL 15 and active layer 107, Fig. 3, paragraphs [0032]+; "substrate" is interpreted broadly) having a plurality of source/drain regions (114, 116, paragraph [0038]), the source/drain regions having a different conductivity type than the remainder of the substrate (as is known in the art);

a nanolaminate gate dielectric (105, paragraph [0038], and note that 105 here is functionally the same as layered layer 5 above) formed over the substrate substantially between the plurality of source/drain regions, the gate dielectric comprising an oxide--nitride--high-k dielectric composition of oxide-nitride- Al_2O_3 (paragraphs [0018] to [0020]), meeting the claimed Markush group of oxide-nitride-Al_2O_3 and oxide-nitride-HfO_2; and

a control gate (103) formed over the gate dielectric.

Referring to **claim 36**, the reference further discloses that the control gate (3) is a polysilicon material (paragraph [0027]).

Referring to **claims 38-40**, the limitations "fabricated using atomic layer deposition", "fabricated using an evaporation technique", and fabricated using a combination of an atomic layer deposition and an evaporation technique" are taken to be product-by-process limitations and considered non-limitation in a product claim (MPEP 2112.01 and MPEP 2113).

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. **Claims 35, 37, and 41-44** are rejected under 35 U.S.C. §103(a) as being unpatentable over Sadd et al. U.S. Patent Application Publication 20020076850 (hereinafter the '850 reference).

Referring to **claims 41 and 44**, the '850 reference discloses an NROM memory transistor as claimed and as detailed above for claim 1, but does not teach that the NROM memory transistor could be formed as a memory array including an array of the NROM memory transistors, and further does not teach that the memory array could be used in an electronic system including a processor and a memory device. However, as the reference also does not exclude such usage, such utilization of the NROM memory transistor in an array and eventually in an electronic system would have been obvious to one of ordinary skill in the art at the time the invention was made.

Referring to **claim 43**, the reference further discloses that the substrate is silicon (paragraph [0012]) and the control gate is a polysilicon material (paragraph [0016]).

Referring to **claims 35, 37, and 42**, although the reference does not disclose that the source/drain regions are comprised of n+ type doped silicon (silicon doped with a negative+ conductivity type) and that the substrate is comprised of p-type silicon (silicon doped with a positive- conductivity type, a conductivity type opposite to the conductivity type used by the source/drain regions), it is known in the art that source/drain regions are comprised of a first conductivity type and that the substrate is comprised of second conductivity type opposite to the conductivity type used by the source/drain regions, therefore such selection of conductivity types would have been obvious.

7. **Claims 35, 37, and 42-44** are rejected under 35 U.S.C. §103(a) as being unpatentable over Mahajani et al. U.S. Patent Application Publication 20040069990 (hereinafter the '990 reference).

Referring to **claim 44**, the '990 reference discloses an NROM memory transistor as claimed and as detailed above for claims 1 and 41, but does not teach that the NROM memory array including an array of the NROM memory transistors could be used in an electronic system including a processor and a memory device. However, as the reference also does not exclude such usage, such utilization of the NROM memory array in an electronic system would have been obvious to one of ordinary skill in the art at the time the invention was made.

Referring to **claim 43**, the reference further discloses that the control gate is a polysilicon material (paragraph [0027]).

Referring to **claims 37 and 43**, although the reference does not teach that the substrate is or comprises silicon, the reference discloses that the substrate is semiconductor (paragraph

[0015]); and because at the time the invention was made silicon was widely used as a semiconductor material and because the reference does not exclude such usage, using silicon as a semiconductor material for the semiconductor substrate would have been obvious to one of ordinary skill in the art and such selection of known and available material for its intended use should not contribute to patentability.

Referring to **claims 35, 37, and 42**, although the reference does not disclose that the source/drain regions are comprised of n+ type doped silicon (silicon doped with a negative+ conductivity type) and that the substrate is comprised of p-type silicon (silicon doped with a positive- conductivity type, a conductivity type opposite to the conductivity type used by the source/drain regions), it is known in the art that source/drain regions are comprised of a first conductivity type and that the substrate is comprised of second conductivity type opposite to the conductivity type used by the source/drain regions, therefore such selection of conductivity types would have been obvious.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office Action. See MPEP § 706.07(a).

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TH

Tu-Tu Ho
October 21, 2005